

University of Illinois at Urbana-Champaign
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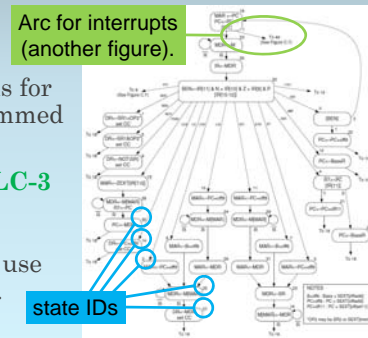
ECE 120: Introduction to Computing

The Patt and Patel Control Unit

LC-3 State Transition Diagram Has Few Outgoing Arcs

Patt and Patel Appendix C provides details for a microprogrammed control unit.

Since the full **LC-3 ISA** includes interrupts and privilege, they use 6-bit state IDs.



Microprogrammed Control Treats States as Instructions

Interrupts and privilege add 14 bits of control signals, bringing the total to 39.

The P&P microinstructions also include 10 bits of sequencing information:

- **J**, a 6-bit next state ID
- **COND**, a 3-bit branch condition,
- and **IRD**, which indicates whether the current state is the decode state (#32).

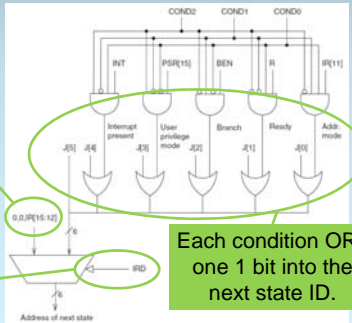
Microinstruction Branch Conditions for LC-3

| COND | branch on signal | meaning |
|------|------------------|---------------------------|
| 000 | (none) | unconditional |
| 001 | R | memory ready |
| 010 | BEN | BR taken |
| 011 | IR[11] | JSR or JSRR |
| 100 | PSR[15] | privilege mode violation |
| 101 | INT | interrupt occurred |

Grey entries were not covered in our class.

The Patt and Patel Microsequencer

Here is the P&P microsequencer.



First states of execution are 0 through 15.

Decode is handled using IRD.

Each condition ORs one 1 bit into the next state ID.

Microsequencer Constrains the Choice of State Numbers

For example, the memory ready signal **R** ORs in the value 2 (bit #1).

To wait for a memory access:

- **COND** must be 001.
- The current state ID must have **bit 1 = 0**.
- Next state **J** must be the same as current state.
- Next state after memory is ready must be **J + 2 (J OR 2)**, which is the same as +).

These **constraints must be obeyed** because of the microsequencer design.

Consider the BR Instruction as an Example

Let's look at an example.

The **BR** opcode is 0, so the **BR** execution state is also #0.

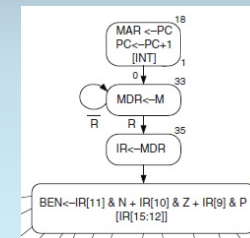
State #0 branches on **BEN**:

- when **BEN** is false, the branch is not taken, so the next state is fetch (#18), and
- when **BEN** is true, the next state must be #22 (18 OR 4), as the microsequencer ORs 4 with **J** when **COND = 2** and **BEN = 1**.

How Does the LC-3 FSM Control Fetch and Decode?

Let's work out the microsequencing bits for instruction fetch and decode.

The figure to the right highlights these states.



What are the Microsequencing Bits for Fetch 1?

Fetch 1 branches on **INT** (interrupt).

The next states are fetch 2 (100001) and start of interrupt (110001).

| state # | | J | COND | IRD |
|---------|---------|--------|------|-----|
| 010010 | fetch 1 | 100001 | 101 | 0 |
| 100001 | fetch 2 | | | |
| 100011 | fetch 3 | | | |
| 100000 | decode | | | |

What are the Microsequencing Bits for Fetch 2?

Fetch 2 branches on **R** (memory ready).

The next states are fetch 2 (100001) and fetch 3 (100011).

| state # | | J | COND | IRD |
|---------|---------|--------|------|-----|
| 010010 | fetch 1 | 100001 | 101 | 0 |
| 100001 | fetch 2 | 100001 | 001 | 0 |
| 100011 | fetch 3 | | | |
| 100000 | decode | | | |

What are the Microsequencing Bits for Fetch 3?

Fetch 3 does not branch.

The next state is decode (100000).

| state # | | J | COND | IRD |
|---------|---------|--------|------|-----|
| 010010 | fetch 1 | 100001 | 101 | 0 |
| 100001 | fetch 2 | 100001 | 001 | 0 |
| 100011 | fetch 3 | 100000 | 000 | 0 |
| 100000 | decode | | | |

What are the Microsequencing Bits for Decode?

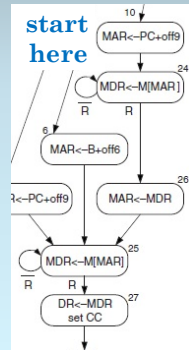
Decode goes to a state from 000000 to 001111, depending on the opcode **IR[15:12]**.

| state # | | J | COND | IRD |
|---------|---------|---------|------|-----|
| 010010 | fetch 1 | 100001 | 101 | 0 |
| 100001 | fetch 2 | 100001 | 001 | 0 |
| 100011 | fetch 3 | 100000 | 000 | 0 |
| 100000 | decode | xxxxxxx | xxx | 1 |

How Does the LC-3 FSM Control LDI Execution?

Let's work out the microsequencing bits for executing an **LDI** instruction.

The figure to the right highlights these states.



What are the Microsequencing Bits for LDI1?

LDI1 does not branch.

The next state is LDI2 (011000).

| state # | | J | COND | IRD |
|---------|------|--------|------|-----|
| 001010 | LDI1 | 011000 | 000 | 0 |
| 011000 | LDI2 | | | |
| 011010 | LDI3 | | | |
| 011001 | LDI4 | | | |
| 011011 | LDI5 | | | |

What are the Microsequencing Bits for LDI2?

LDI2 branches on **R** (memory ready).

The next states are LDI2 (011000) and LDI3 (011010).

| state # | | J | COND | IRD |
|---------|------|--------|------|-----|
| 001010 | LDI1 | 011000 | 000 | 0 |
| 011000 | LDI2 | 011000 | 001 | 0 |
| 011010 | LDI3 | | | |
| 011001 | LDI4 | | | |
| 011011 | LDI5 | | | |

What are the Microsequencing Bits for LDI3?

LDI3 does not branch.

The next state is LDI4 (011001).

| state # | | J | COND | IRD |
|---------|------|--------|------|-----|
| 001010 | LDI1 | 011000 | 000 | 0 |
| 011000 | LDI2 | 011000 | 001 | 0 |
| 011010 | LDI3 | 011001 | 000 | 0 |
| 011001 | LDI4 | | | |
| 011011 | LDI5 | | | |

What are the Microsequencing Bits for LDI4?

LDI4 branches on **R** (memory ready).

The next states are LDI4 (011001) and LDI5 (011011).

| state # | | J | COND | IRD |
|---------|------|--------|------|-----|
| 001010 | LDI1 | 011000 | 000 | 0 |
| 011000 | LDI2 | 011000 | 001 | 0 |
| 011010 | LDI3 | 011001 | 000 | 0 |
| 011001 | LDI4 | 011001 | 001 | 0 |
| 011011 | LDI5 | | | |

What are the Microsequencing Bits for LDI5?

LDI5 does not branch.

The next state is fetch 1 (010010).

| state # | | J | COND | IRD |
|---------|------|--------|------|-----|
| 001010 | LDI1 | 011000 | 000 | 0 |
| 011000 | LDI2 | 011000 | 001 | 0 |
| 011010 | LDI3 | 011001 | 000 | 0 |
| 011001 | LDI4 | 011001 | 001 | 0 |
| 011011 | LDI5 | 010010 | 000 | 0 |