University of Illinois at Urbana-Champaign
Dept. of Electrical and Computer Engineering

ECE 120: Introduction to Computing

LC-3 Control Signals for Execution of an LDI

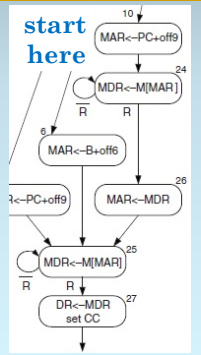
How Does the LC-3 FSM Control LDI Execution?

Let's work out the control signals needed for executing an **LDI** instruction.

The figure to the right is part of Patt and Patel Figure C.2.

The first state:

MAR ← PC + off9



What are the Load Signals?

MAR ← PC + off9

Which registers change?

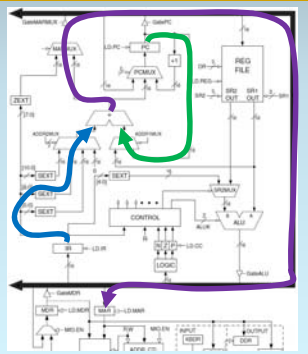
	LD. MAR	LD. MDR	LD. IR	LD. BEN	LD. REG	LD. CC	LD. PC
LDI1	1	0	0	0	0	0	0
LDI2							
LDI3							
LDI4							
LDI5							

Look at How Bits Must Move in the Datapath

Let's look at the datapath.

We have…

MAR ← PC + off9



What are the Bus Gating Signals?

MAR ← PC + off9

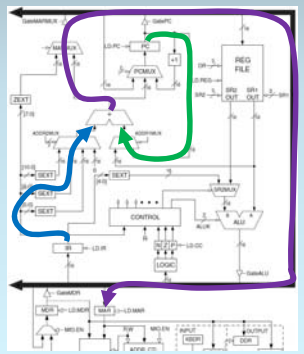
So what are the bus gating signals?

	GatePC	GateMDR	GateALU	Gate MARMUX
LDI1	0	0	0	1
LDI2				
LDI3				
LDI4				
LDI5				

Which Muxes are Needed for LDI1?

Which muxes matter?

The three address generation muxes (ADDR1MUX, ADDR2MUX, and MARMUX).



What are the Mux Selection Signals?

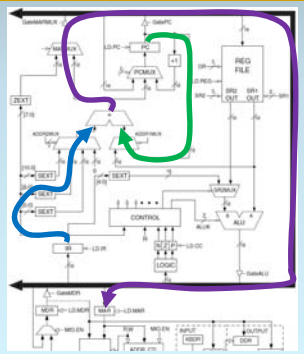
MAR ← PC + off9

What are the mux selection signals?

	PC MUX	DR MUX	SR1 MUX	ADDR1 MUX	ADDR2 MUX	MAR MUX
LDI1	xx	xx	xx	0	10	1
LDI2						
LDI3						
LDI4						
LDI5						

The LDI1 State Uses Neither the ALU nor Memory

Both the **ALU** and memory are unused.



What are the ALU and Memory Signals?

MAR ← PC+ off9

What are the ALU and memory signals?

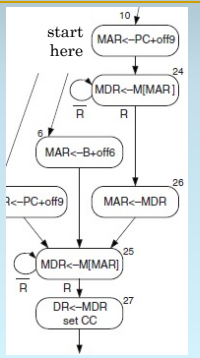
	ALUK	MIO.EN	R.W
LDI1	xx	0	x
LDI2			
LDI3			
LDI4			
LDI5			

Continue with the Second LDI Execution State

Identical to the second fetch state's RTL, so we'll copy the control signals!

The second LDI state:

MDR ← M[MAR]



What are the Load Signals?

MDR ← M[MAR]

Which registers change?

	LD. MAR	LD. MDR	LD. IR	LD. BEN	LD. REG	LD. CC	LD. PC
LDI1	1	0	0	0	0	0	0
LDI2	0	1	0	0	0	0	0
LDI3							
LDI4							
LDI5							

What are the Bus Gating Signals?

MDR ← M[MAR]

What are the bus gating signals?

	GatePC	GateMDR	GateALU	Gate MARMUX
LDI1	0	0	0	1
LDI2	0	0	0	0
LDI3				
LDI4				
LDI5				

What are the Mux Selection Signals?

MDR ← M[MAR]

What are the mux selection signals?

	PC MUX	DR MUX	SR1 MUX	ADDR1 MUX	ADDR2 MUX	MAR MUX
LDI1	xx	xx	xx	0	10	1
LDI2	xx	xx	xx	x	xx	x
LDI3						
LDI4						
LDI5						

What are the ALU and Memory Signals?

MDR ← M[MAR]

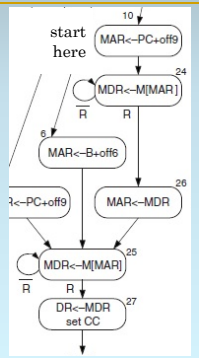
What are the ALU and memory signals?

	ALUK	MIO.EN	R.W
LDI1	xx	0	x
LDI2	xx	1	0
LDI3			
LDI4			
LDI5			

Continue with the Third LDI Execution State

The third LDI state:

MAR ← MDR



What are the Load Signals?

MAR ← MDR

Which registers change?

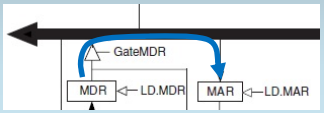
	LD. MAR	LD. MDR	LD. IR	LD. BEN	LD. REG	LD. CC	LD. PC
LDI1	1	0	0	0	0	0	0
LDI2	0	1	0	0	0	0	0
LDI3	1	0	0	0	0	0	0
LDI4							
LDI5							

Look at How Bits Must Move in the Datapath

Let's look at the datapath.

We have…

MAR ← MDR



What are the Bus Gating Signals?

MAR ← MDR

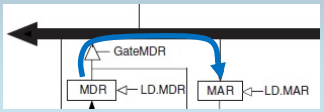
What are the bus gating signals?

	GatePC	GateMDR	GateALU	Gate MARMUX
LDI1	0	0	0	1
LDI2	0	0	0	0
LDI3	0	1	0	0
LDI4				
LDI5				

Which Muxes are Needed for LDI3?

Which muxes matter?

None of them!



What are the Mux Selection Signals?

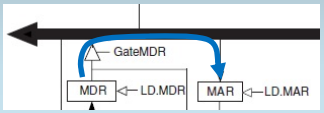
MAR ← MDR

What are the mux selection signals?

	PC MUX	DR MUX	SR1 MUX	ADDR1 MUX	ADDR2 MUX	MAR MUX
LDI1	xx	xx	xx	0	10	1
LDI2	xx	xx	xx	x	xx	x
LDI3	xx	xx	xx	x	xx	x
LDI4						
LDI5						

The LDI3 State Uses Neither the ALU nor Memory

Both the **ALU** and memory are unused.



What are the ALU and Memory Signals?

MAR ← MDR

What are the ALU and memory signals?

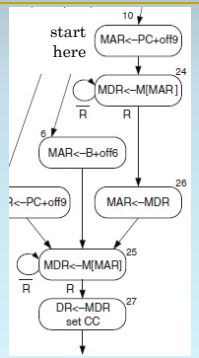
	ALUK	MIO.EN	R.W
LDI1	xx	0	x
LDI2	xx	1	0
LDI3	xx	0	x
LDI4			
LDI5			

Continue with the Fourth LDI Execution State

Identical to LDI2, so we'll copy the control signals!

The fourth LDI state:

MDR ← M[MAR]



What are the Load Signals?

MDR ← M[MAR]

Which registers change?

	LD. MAR	LD. MDR	LD. IR	LD. BEN	LD. REG	LD. CC	LD. PC
LDI1	1	0	0	0	0	0	0
LDI2	0	1	0	0	0	0	0
LDI3	1	0	0	0	0	0	0
LDI4	0	1	0	0	0	0	0
LDI5							

What are the Bus Gating Signals?

MDR ← M[MAR]

What are the bus gating signals?

	GatePC	GateMDR	GateALU	Gate MARMUX
LDI1	0	0	0	1
LDI2	0	0	0	0
LDI3	0	1	0	0
LDI4	0	0	0	0
LDI5				

What are the Mux Selection Signals?

MDR ← M[MAR]

What are the mux selection signals?

	PC MUX	DR MUX	SR1 MUX	ADDR1 MUX	ADDR2 MUX	MAR MUX
LDI1	xx	xx	xx	0	10	1
LDI2	xx	xx	xx	x	xx	x
LDI3	xx	xx	xx	x	xx	x
LDI4	xx	xx	xx	x	xx	x
LDI5						

What are the ALU and Memory Signals?

MDR ← M[MAR]

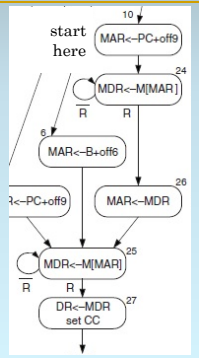
What are the ALU and memory signals?

	ALUK	MIO.EN	R.W
LDI1	xx	0	x
LDI2	xx	1	0
LDI3	xx	0	x
LDI4	xx	1	0
LDI5			

Continue with the Fifth LDI Execution State

The fifth LDI state:

DR ← MDR, set CC



What are the Load Signals?

DR ← MDR, set CC

Which registers change?

	LD. MAR	LD. MDR	LD. IR	LD. BEN	LD. REG	LD. CC	LD. PC
LDI1	1	0	0	0	0	0	0
LDI2	0	1	0	0	0	0	0
LDI3	1	0	0	0	0	0	0
LDI4	0	1	0	0	0	0	0
LDI5	0	0	0	0	1	1	0

Look at How Bits Must Move in the Datapath

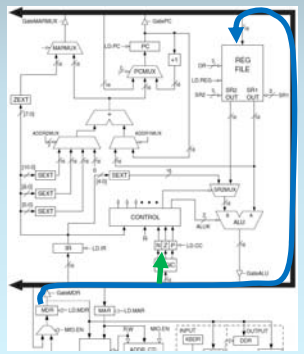
Let's look at the datapath.

We have…

DR ← MDR

and

set CC



What are the Bus Gating Signals?

DR ← MDR, set CC

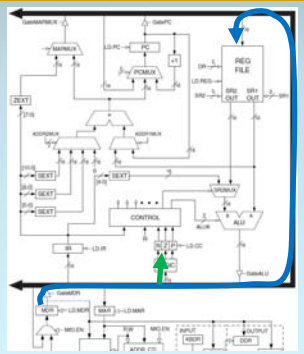
What are the bus gating signals?

	GatePC	GateMDR	GateALU	Gate MARMUX
LDI1	0	0	0	1
LDI2	0	0	0	0
LDI3	0	1	0	0
LDI4	0	0	0	0
LDI5	0	1	0	0

Which Muxes are Needed for LDI5?

Which muxes matter?

Only DRMUX.



What are the Mux Selection Signals?

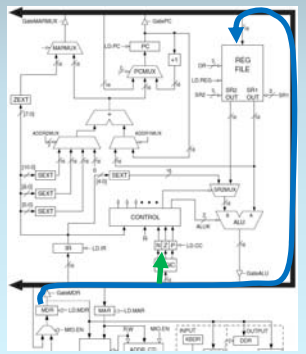
DR ← MDR, set CC

What are the mux selection signals?

	PC MUX	DR MUX	SR1 MUX	ADDR1 MUX	ADDR2 MUX	MAR MUX
LDI1	xx	xx	xx	0	10	1
LDI2	xx	xx	xx	x	xx	x
LDI3	xx	xx	xx	x	xx	x
LDI4	xx	xx	xx	x	xx	x
LDI5	xx	00	xx	x	xx	x

The LDI5 State Uses Neither the ALU nor Memory

Both the **ALU** and memory are unused.



What are the ALU and Memory Signals?

DR ← MDR, set CC

What are the ALU and memory signals?

	ALUK	MIO.EN	R.W
LDI1	xx	0	x
LDI2	xx	1	0
LDI3	xx	0	x
LDI4	xx	1	0
LDI5	xx	0	x

Summary of Control Signals for LDI Execution

	LD. MAR	LD. MDR	LD. IR	LD. BEN	LD. REG	LD. CC	LD. PC
LDI1	1	0	0	0	0	0	0
LDI2	0	1	0	0	0	0	0
LDI3	1	0	0	0	0	0	0
LDI4	0	1	0	0	0	0	0
LDI5	0	0	0	0	1	1	0

	GatePC	GateMDR	GateALU	Gate MARMUX
LDI1	0	0	0	1
LDI2	0	0	0	0
LDI3	0	1	0	0
LDI4	0	0	0	0
LDI5	0	1	0	0

	PC MUX	DR MUX	SR1 MUX	ADDR1 MUX	ADDR2 MUX	MAR MUX
LDI1	xx	xx	xx	0	10	1
LDI2	xx	xx	xx	x	xx	x
LDI3	xx	xx	xx	x	xx	x
LDI4	xx	xx	xx	x	xx	x
LDI5	xx	00	xx	x	xx	x

	ALUK	MIO.EN	R.W
LDI1	xx	0	x
LDI2	xx	1	0
LDI3	xx	0	x
LDI4	xx	1	0
LDI5	xx	0	x

