University of Illinois at Urbana-Champaign
Dept. of Electrical and Computer Engineering

ECE 120: Introduction to Computing

LC-3 Control Signals

Time to Examine a Processor's Control Signals in Detail

Recall the control unit **FSM**
- inputs: signals from the datapath
- outputs: **control signals** for the datapath

Let's look at the **control signals for Patt and Patel's LC-3 datapath** (Figure C.3).

We ignore control signals associated with interrupt and privilege.

Those of you who take ECE391 will cover these concepts in the context of the **x86** ISA.

We Consider Five Groups of LC-3 Control Signals

Let's split the control signals into five groups:
- **register loads**:
  does a register take a new value?
- **bus gating**:
  should a value be copied onto the bus?
- **mux selection**
- **ALU function selection**
- **memory operation**

Register Loads Control Updates to Register Values

The first group: **register loads**.

Each register load signal controls one or more registers.

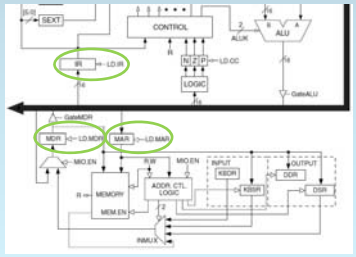
Each signal is **set iff the RTL for the current FSM state changes that register's value**.

In other words, the load signal is
- 1 if the register appears on the left side of an **RTL** expression,
- and is 0 otherwise.

Register Load Signals are Set iff a Register Should Change

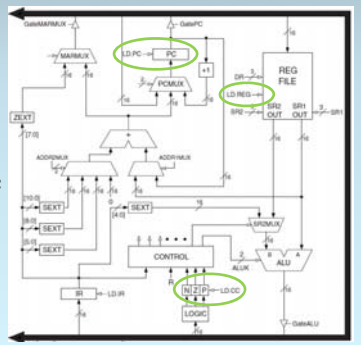
Load signals include:

- **LD.MAR**
- **LD.MDR**
- **LD.IR**
- **LD.BEN** (not shown)



Register Load Signals are Set iff a Register Should Change

- **LD.REG** (register file; which register depends on **DR** input)
- **LD.CC** (all three; logic calculates values based on bits on bus)
- **LD.PC**



What Values Do the Registers Write?

Most registers' new values come **from the bus**: **MAR**, **IR**, **REG**, and **CC**.

MDR's new value comes either from the bus or **from the memory**.

PC's new value comes **from a mux** (**PCMUX**), with one mux input from the bus.

Finally, **BEN** (branch enable) is loaded **based on CC and IR**.

Bus Gating Signals Determine the Value on the Bus

The second group: **bus gating**.

Recall that tri-state buffers are used to write values onto the bus.

Each bus gating control signal is **wired to the enable inputs of 16 tri-state buffers** that write to the bus.

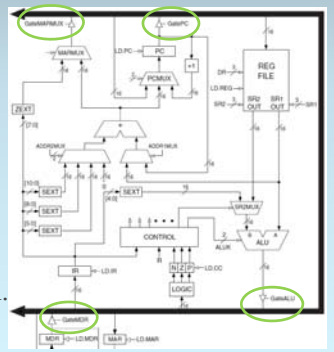
At most one bus gating signal can be a 1.

All others must be 0 to avoid short circuits through the bus.

Bus Gating Signals Determine the Value on the Bus

Bus gating signals include:
- **GatePC**
- **GateMDR**
- **GateALU**
- **GateMARMUX**

MARMUX is used for memory address generation.



Mux Selection Signals Control Mux Outputs

The third group: **mux selection**.

Muxes are used to control
- the value loaded into the **PC**,
- the destination register in the **register file**,
- source register 1 from the register file, and
- memory address generation (three muxes).

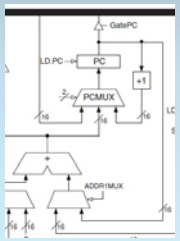
When mux outputs are not used, their select inputs can be don't cares.

PCMUX Controls the Value Loaded into the PC

PCMUX controls the value loaded into the PC, and is thus only meaningful when **LD.PC = 1**.

Choices include:

00	**PC + 1**
01	bus
10	address generation adder (used for **BR** and **JMP**)

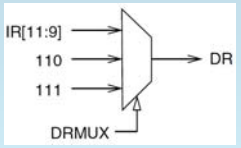


DRMUX Controls the Destination Register

DRMUX controls the destination register, and is thus only meaningful when **LD.REG = 1**.

Choices include:

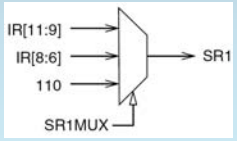
00	**IR[11:9]**
01	**R7**
10	**R6**



The instructions that we covered only make use of the first option.

SR1MUX Controls the First Source Register

SR1MUX controls source register 1 from the register file, which is used by the **ALU** and by **ADDR1MUX**.



Choices include:

00 **IR[11:9]** (stores)

01 **IR[8:6]** (**ALU** ops, **JMP**, **LDR**/**STR**)

10 **R6** (nothing that we have seen)

Two Muxes are Used for the Memory Address Adder

ADDR1MUX selects between

0 **PC**

1 **SR1**

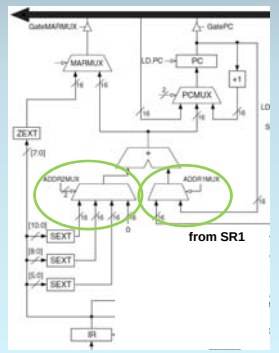
ADDR2MUX selects between

00 **0**

01 **SEXT(IR[5:0])**

10 **SEXT(IR[8:0])**

11 **SEXT(IR[10:0])**



And a Third Mux is Used to Select the Address

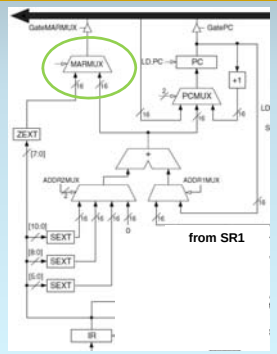
Finally, **MARMUX** selects between

0 **ZEXT(IR[7:0])**

1 address generation adder

The instructions that we explained* use only the second option.

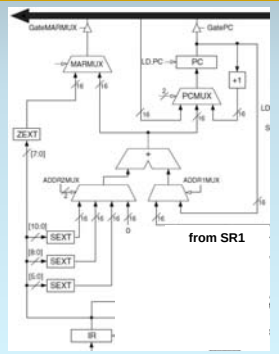
*TRAP's implementation uses the first option.



Address Generation is Not Always Used

Notice that **ADDR1MUX** and **ADDR2MUX** are used by both **PCMUX** and by **MARMUX**.

MARMUX is useful only when **GateMARMUX = 1**.



The LC-3 ALU Supports Four Functions

The fourth group of control signals:
ALU function selection.

The **ALUK** control signals support for functions, including passing the **A** input to the output.

00	**ADD**
01	**AND**
10	**NOT A**
11	PASS **A**

ALUK is meaningful only when **GateALU = 1**.

The LC-3 Memory Requires Two Signals

The fifth group of control signals:
memory operation.

The **LC-3** memory requires two controls:

MIO.EN tells the memory to operate (1 to do a read or a write).

When **MIO.EN = 1**,
- **R.W = 1** for a write, and
- **R.W = 0** for a read.

We Consider Twenty-Five Control Signals in All

How many control signals do we have?

register loads	7
bus gating	4
mux selection	10
ALU function selection	2
memory operation	2
TOTAL	**25**

