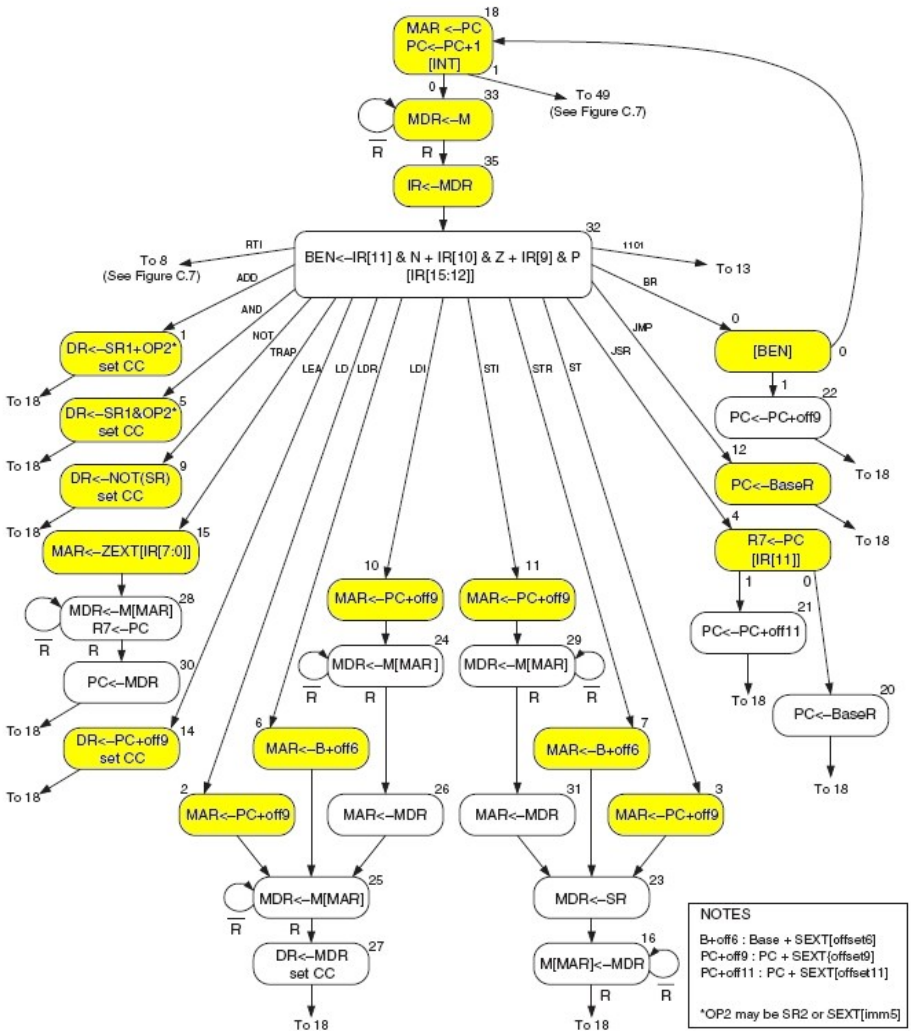


### LC-3 FSM

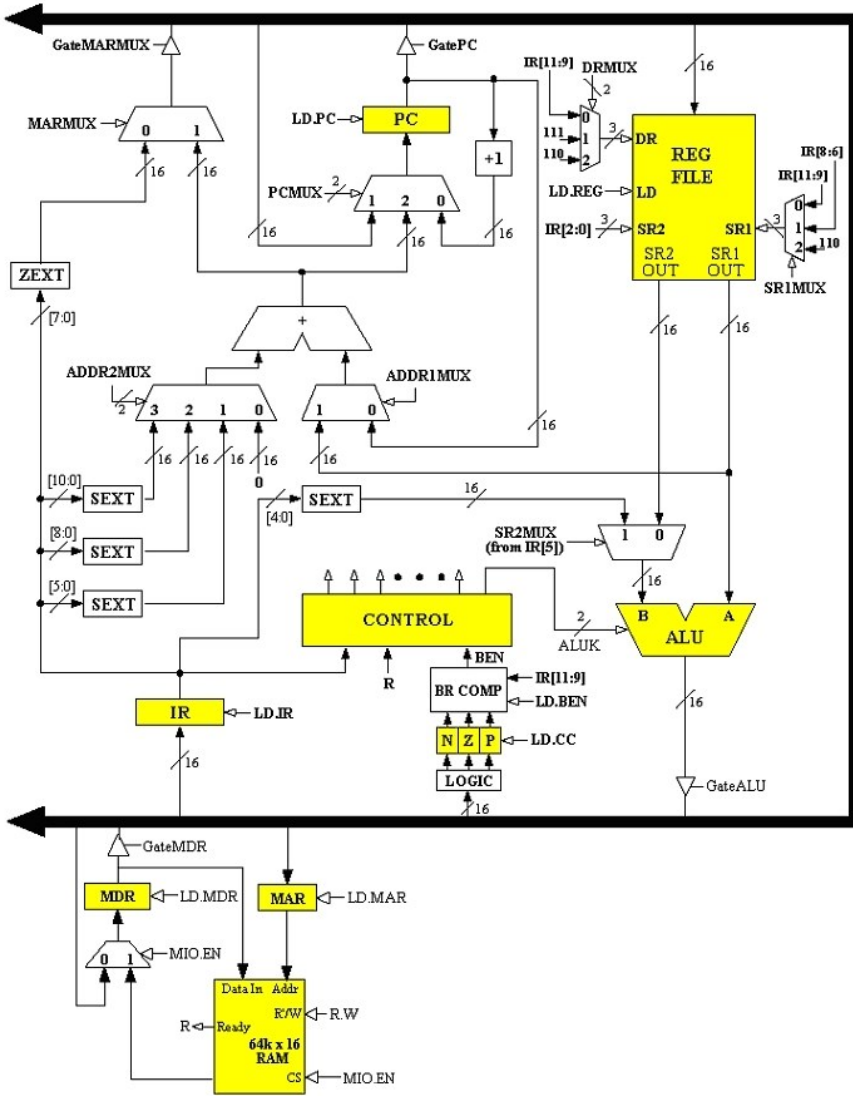


NOTES: RTL corresponds to execution (after fetch!); JSRR not shown

### LC-3 Instructions

ADD 0001 DR SR1 0 00 SR2 DR ← SR1 + SR2, Setcc	ADD DR, SR1, SR2 LD 0010 DR Pcoffset9 DR ← MIPc + SEXT(Pcoffset9), Setcc	LD 0010 DR Pcoffset9 LD DR, Pcoffset9
ADD 0001 DR SR1 1 imm5 DR ← SR1 + SEXT(imm5), Setcc	ADD DR, SR1, imm5 LDI 1010 DR Pcoffset9 DR ← MIMIPc + SEXT(Pcoffset9)], Setcc	LDI 1010 DR Pcoffset9 LDI DR, Pcoffset9
AND 0101 DR SR1 0 00 SR2 DR ← SR1 AND SR2, Setcc	AND DR, SR1, SR2 LDR 0110 DR Baser offset6 DR ← MIBaser + SEXT(offset6)], Setcc	LDR 0110 DR Baser offset6 LDR DR, Baser, offset6
AND 0101 DR SR1 1 imm5 DR ← SR1 AND SEXT(imm5), Setcc	AND DR, SR1, imm5 LEA 1110 DR Pcoffset9 DR ← PC + SEXT(Pcoffset9), Setcc	LEA 1110 DR Pcoffset9 LEA DR, Pcoffset9
BR 0000 n z p Pcoffset9 (n AND N) OR (z AND Z) OR (p AND P): PC ← PC + SEXT(Pcoffset9)	BR(nzp) Pcoffset9 NOT 1001 DR SR 111111 DR ← NOT SR, Setcc	NOT 1001 DR SR 111111 NOT DR, SR
JMP 1100 000 Baser 000000 PC ← Baser	JMP Baser ST 0011 SR Pcoffset9 MIPc + SEXT(Pcoffset9) ← SR	ST 0011 SR Pcoffset9 ST SR, Pcoffset9
JSR 0100 1 Pcoffset11 R7 ← PC, PC ← PC + SEXT(Pcoffset11)	JSR Pcoffset11 STI 1011 SR Pcoffset9 MIMIPc + SEXT(Pcoffset9)] ← SR	STI 1011 SR Pcoffset9 STI SR, Pcoffset9
TRAP 1111 0000 trapvect8 R7 ← PC, PC ← MIZEXT(trapvect8)]	TRAP trapvect8 STR 0111 SR Baser offset6 MIBaser + SEXT(offset6) ← SR	STR 0111 SR Baser offset6 STR SR, Baser, offset6

## LC-3 Datapath



## LC-3 Datapath Control Signals

Signal	Description	Signal	Description
LD.MAR	= 1, MAR is loaded	LD.CC	= 1, updates status bits from system bus
LD.MDR	= 1, MDR is loaded	GateMARMUX	= 1, MARMUX output is put onto system bus
LD.IR	= 1, IR is loaded	GateMDR	= 1, MDR contents are put onto system bus
LD.PC	= 1, PC is loaded	GateALU	= 1, ALU output is put onto system bus
LD.REG	= 1, register file is loaded	GatePC	= 1, PC contents are put onto system bus
LD.BEN	= 1, updates Branch Enable (BEN) bit	MIO.EN	= 1, Enables memory, = 0, Disables memory, = 10, chooses system bus for MDR input
MARMUX	= 0, chooses ZEXT IR[7:0] = 1, chooses address adder output	R.W	= 1, M[MAR]<-MDR when MIO.EN = 1 = 0, MDR<-M[MAR] when MIO.EN = 1
ADDR1MUX	= 0, chooses PC + 1 = 01, chooses system bus = 10, chooses address adder output	ALUK	= 00, ADD = 01, AND = 10, NOT A = 11, PASS A
ADDR2MUX	= 00, chooses "0...00" = 01, chooses SEXT IR[5:0] = 10, chooses SEXT IR[8:0] = 11, chooses SEXT IR[10:0]	DRMUX	= 00, chooses IR[11:9] = 01, chooses "11" = 10, chooses "110"
PCMUX	= 00, chooses PC + 1 = 01, chooses system bus = 10, chooses address adder output		
SR1MUX	= 00, chooses IR[11:9] = 01, chooses IR[8:6] = 10, chooses "110"		